

## Getting the Most from High Resolution D/A Converters

by Scott Wayne

Here's a close look at D/A converter specs, requirements, error sources, and test methods—and how they can affect your circuit designs

**H**igh resolution digital-to-analog converters have many varied applications that can be loosely grouped into two categories: instrumentation and waveform reconstruction. Instrumentation applications include raster scan, process control, automatic test equipment, robotics, and others. Waveform reconstruction includes digital audio, sonar, and telecommunications, as well as specialized waveform generation. Each of these two classifications has widely different specifications and requirements for D/A converters. For example, instrumentation applications require traditional D/A specifications such as good linearity and high stability, while waveform reconstruction applications require low total harmonic distortion (THD) and a high signal-to-noise ratio (S/N).

### D/A converter for instrumentation

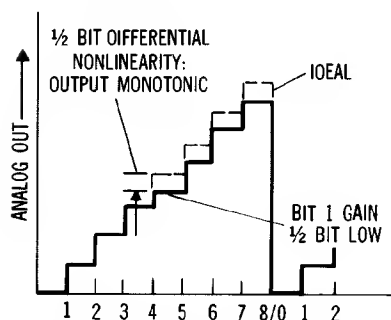
A high-resolution D/A converter for instrumentation must have low differential nonlinearity (DNL) and integral nonlinearity (INL) over

temperature. It also must have low offset and gain drift, a high power supply rejection ratio (PSRR), and low noise. This explanation of the more important instrumentation specifications — as well as techniques for measuring and improving them — should prove helpful in applying high-resolution D/As.

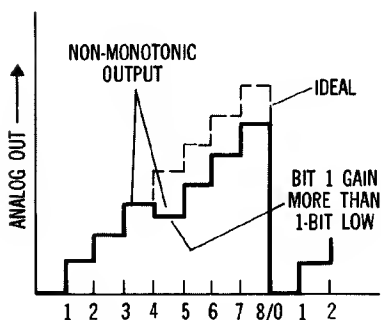
As the digital input to a D/A converter changes by one bit, the analog output changes by some amount. Ideally, a one bit digital input change should produce a constant 1 LSB (least significant bit) output change anywhere along the input-output transfer function. Differential nonlinearity, usually the most important specification for an instrumentation converter, is a measure of the deviation between the actual analog output change and the theoretical change of 1 LSB. It is specified at room temperature in LSBs or as a percentage of full scale range (FSR). Differential nonlinearity is a function of time and temperature. Its drift is given in ppm 1000 hours or ppm/°C.

Monotonicity is another measure of differential nonlinearity. If a converter is monotonic, the analog output will remain constant or increase as the digital input is increased. Nonmonotonicity implies a differential linearity error of greater than 1 LSB. To compute the monotonic temperature range of a converter, subtract the initial differential nonlinearity of the D/A from 1 LSB. Divide the result by the DNL drift temperature coefficient. This gives the minimum temperature deviation around room temperature for which the converter will remain monotonic. For example, given a 16-bit device with an initial linearity error of  $\frac{1}{2}$  LSB (30 ppm) and a linearity drift of 1 ppm/°C, the monotonic temperature range is 25°C to  $\pm 30^\circ\text{C}$  or  $-5$  to  $+55^\circ\text{C}$ . Monotonicity is a very important specification for process control applications because a nonmonotonic converter will cause the control loop to oscillate endlessly.

Differential nonlinearity can eas-



(a) Differential nonlinearity



(b) Non-monotonicity

Fig. 1. Differential linearity and monotonicity errors

ily be measured by directly comparing the analog output produced by one digital input and the analog output produced by the next sequential digital input. The effects of differential nonlinearity and non-monotonicity errors are shown in Fig. 1.

### Measuring integral nonlinearity

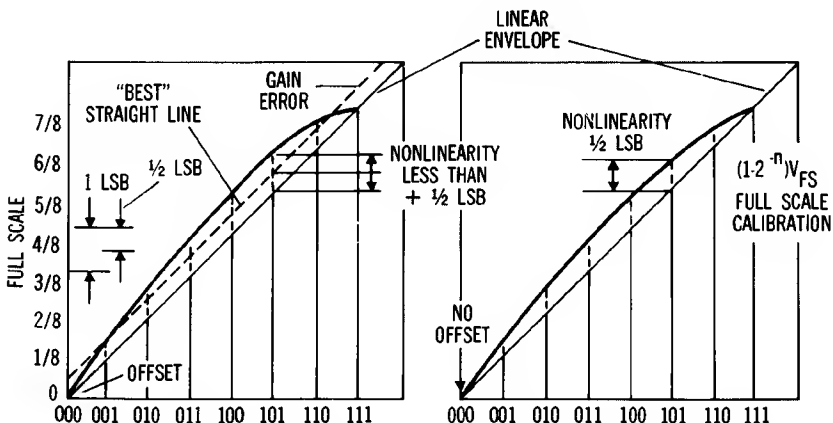
Integral nonlinearity (INL), also referred to as nonlinearity or relative accuracy, is the deviation of the actual converter output from a straight line drawn between the end points of the converter's input-output transfer function (see Fig. 2). INL is very difficult to measure as the measurement involves finding the difference between two large numbers. A  $6\frac{1}{2}$ -digit voltmeter that is accurate to better than 0.0002% would be necessary to accurately measure the integral nonlinearity of a 16-bit converter. For this reason, most integral nonlinearity measurements are made by comparing the converter under test to a reference converter of known accuracy. The errors are then read with a null meter. A precision 18-bit converter can be used to test converters with up to 16-bit accuracy. A precision divider, traceable to the National Bureau of Standards, must be used to properly test an 18-bit converter.

Summation errors, or superposition errors, occur whenever the ana-

log output due to any digital bit combination does not equal the algebraic sum of the analog outputs due to each digital input bit alone. The numerous sources of summation error in D/A converters depend primarily upon their internal architecture. For example, in a typical R-2R ladder configuration, if both outputs are not at the same potential, summation errors will occur. This can easily be seen in the case of the 2-bit converter shown in Fig. 3. Also, if the switch resistance is not the same in both the on and the off positions, summation errors will again occur.

Another cause of summation errors is the feedback resistor in a voltage-output converter. As the analog output increases from zero to full scale, the power dissipated by the feedback resistor increases, and the resistor heats up. This causes a change in resistor value, and a corresponding gain change along the transfer function. Since this apparent gain is different for a sum of bits than it is for the individual bits alone, a summation error occurs. Gain changes are especially troublesome in hybrid and monolithic converters, where the power dissipation of the feedback resistor is limited by its small size.

The simplest method for measuring differential nonlinearity is to



(a)  $\frac{1}{2}$  LSB nonlinearity achieved by arbitrary location of "best straight line."

(b) Nonlinearity reference is straight line through end points.

Fig. 2. Comparison of linearity criteria for 3-bit D/A converter (straight line through end points is easier to measure and gives a more conservative specification)

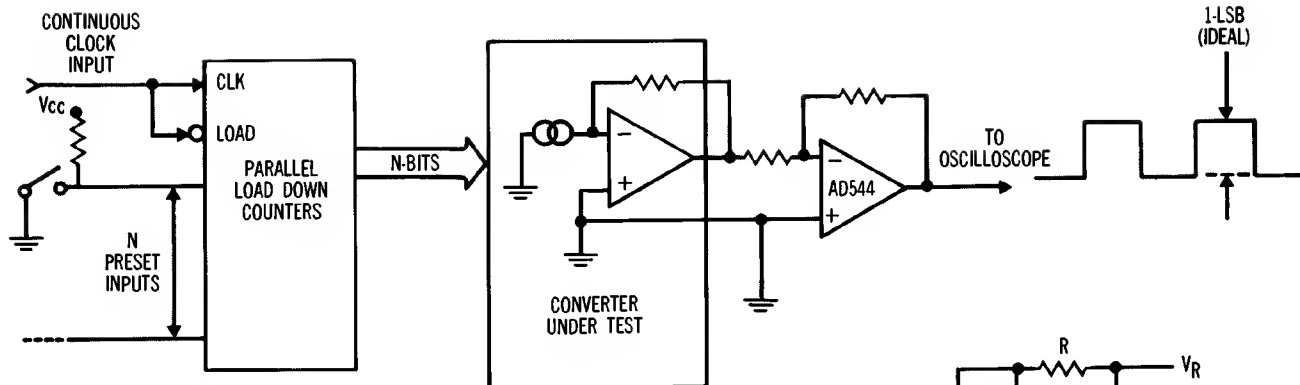


Fig. 4. A simple DNL tester

connect a parallel-load down counter to the device under test (see Fig. 4). The inputs to the counter are first preset to the initial desired digital input value. When the clock goes low, the digital input is asynchronously loaded into the counter, and presented to the converter. The counter counts down by one on the rising edge of the clock pulse, and a digital input value one bit less than the preset input is presented to the converter. Ideally, with a continuous clock signal applied to the counter, the resulting analog output will be a square wave with an amplitude of 1 LSB for any digital input. The deviation of this amplitude from 1 LSB is the differential nonlinearity at the digital input being observed. Amplification of the analog output may be added if desired.

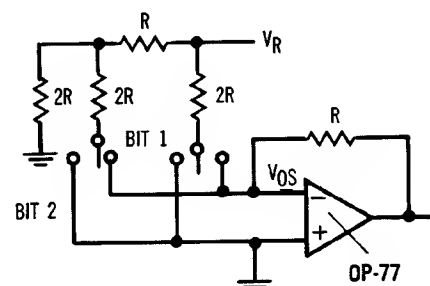
For 18-bit converters, there are  $2^N$  or 262,144 possible digital input combinations. It would be quite tedious to set this many input combinations with toggle switches. Even with an automated tester that required as little as 10 ms per test, the entire sequence would take almost one hour. Fortunately, it is not necessary to test all input combinations to characterize a high resolution device with no summation errors — a total of only  $N$  tests is required. If the summation errors are found to be reasonably small, a total of  $2N$  tests may be sufficient. These tests are usually performed at the major carries, the transitions between a test bit "ON" and all of the bits less significant than the test bit ON, and the test bit OFF.

A simple method for measuring

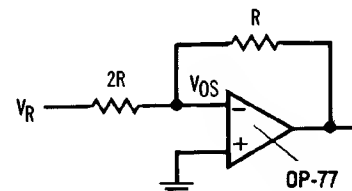
integral nonlinearity is to connect the converter to a parallel-load right-left shift register (see Fig. 5). The register is preset with 00...01. As long as the MSB is a zero, zeroes are shifted in from the right. When the high bit reaches the MSB, ones are shifted in from the left. When the register reaches 11...11 it is again preset and the process continues. A reference converter of at least two bits more accuracy than the one under test is connected to the same register. The two analog outputs are then subtracted and amplified by an instrumentation amplifier. The output of the amplifier is ideally zero volts. The deviation of the output from zero volts is the integral nonlinearity of the converter under test. Zero and gain servos can also be added to enhance this test.

### Program the measurements

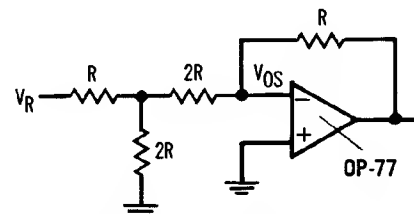
A practical method for simultaneously measuring both integral and differential nonlinearity is to program the desired digital inputs into a PROM (see Fig. 6). As the PROM is cycled, the converter under test undergoes a transition from a single input bit ON alone to all of the lesser significant bits ON, while the input of the reference converter sees just the single bit ON. Each time the lesser significant bits are ON, one LSB of current is added to the output of the converter under test. The two analog outputs are differenced, amplified, and displayed. Ideally, the output of the amplifier is zero volts. The deviation of the output voltage due to each input is



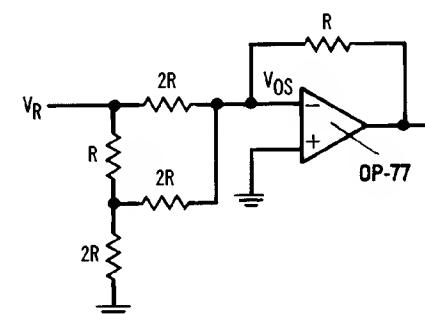
(a) Two bit voltage output R-2R ladder D/A converter



(b) Bit 1 ON,  $V_O = -V_R/2 + 3/2 V_{OS}$



(c) Bit 2 ON,  $V_O = -V_R/4 + 11/8 V_{OS}$



(d) Bits 1 and 2 ON,  $V_O = -3/4 V_R + 15/8 V_{OS} \neq \sum 1+2$

Fig. 3. Summation errors in a 2-bit D/A converter

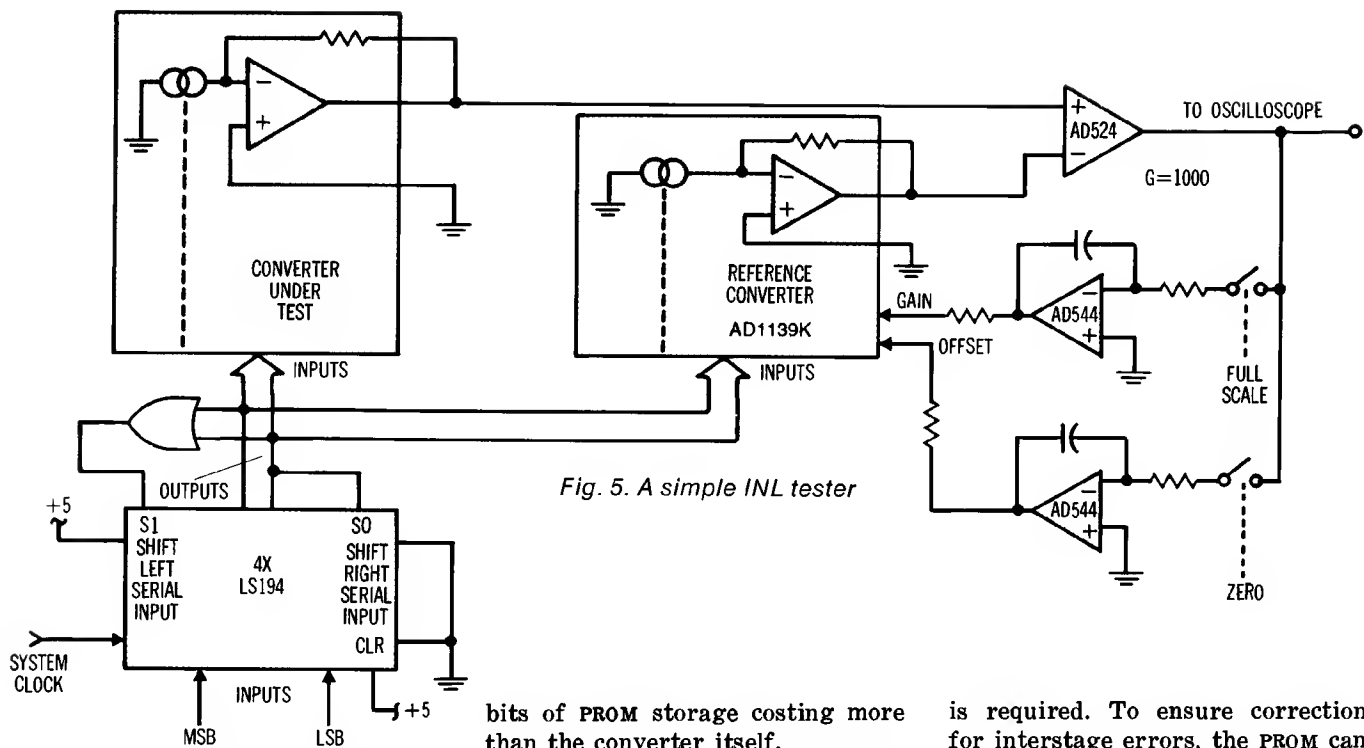


Fig. 5. A simple INL tester

the integral nonlinearity. The difference in output voltage due to adjacent digital inputs is the differential nonlinearity.

This test can easily be automated by replacing the PROM with a microprocessor and using a bus-interfaceable voltmeter in place of the oscilloscope. For each digital input, the output voltage of the amplifier is measured and recorded. This voltage represents the integral nonlinearity. The meter is then nulled, and the digital inputs switched. Output voltage is again measured and recorded to determine the differential nonlinearity. Digital inputs are again switched and the process is repeated until the test is complete.

To improve the linearity of a D/A converter, the error voltage due to each digital input must first be measured. A corresponding correction signal can then be added by a lower resolution converter with a full scale value worth only a few LSBs of the device to be corrected. The input to the correction converter is stored in a PROM that is addressed by the LSBs of a common input bus. While this approach works theoretically, correcting an 18-bit resolution converter from 16-bit to 18-bit accuracy would require 256K x 8-

bits of PROM storage costing more than the converter itself.

For a converter with no summation errors, the worst case integral linearity error will be less than or equal to half of the worst case differential linearity error. Therefore, if the summation errors and the differential linearity errors of a converter are corrected, the integral linearity errors will be corrected also. This means that instead of correcting every possible input, relatively few corrections can be made giving the same net result.

### Suppressing summation errors

Many high resolution converters are composed of several independent internal stages of 4, 8, or 12-bits. The internal architecture can guarantee that these stages don't interact. Therefore, they cannot produce summation errors. Summation errors in the less significant stages may be suppressed with respect to full scale to the extent that they may be neglected. Information about the size and location of the summation errors for any given converter must be determined experimentally.

The only summation errors that are greater than  $\frac{1}{4}$  LSB at 18 bits occur in the four most significant bits. To correct for all of the summation errors, only a 16 x 8 PROM

is required. To ensure correction for interstage errors, the PROM can be increased to 32 x 8 — still many orders of magnitude less than a full correction scheme. The only remaining task is to correct for the differential linearity errors in the 13 lesser significant bits. The net result is equivalent to an 18-bit accurate D/A converter.

A semiautomated calibration scheme is shown in Fig. 7. The analog output due to each digital input to be corrected is compared to the output due to the digital input one bit smaller. One LSB of current is added to the output during the smaller input. The correction converter's input is incremented until the correct analog output is obtained. This input value is stored in RAM. The lesser significant bits are corrected in a similar manner, substituting trimming potentiometers for the correction converter.

### Instrumentation applications

Instrumentation applications for high resolution D/A converters are numerous and varied. Many of these applications use the converter as a programmable voltage source. If the converter has a current output, it can also be used as a programmable current source. Careful note must be taken of the voltage com-

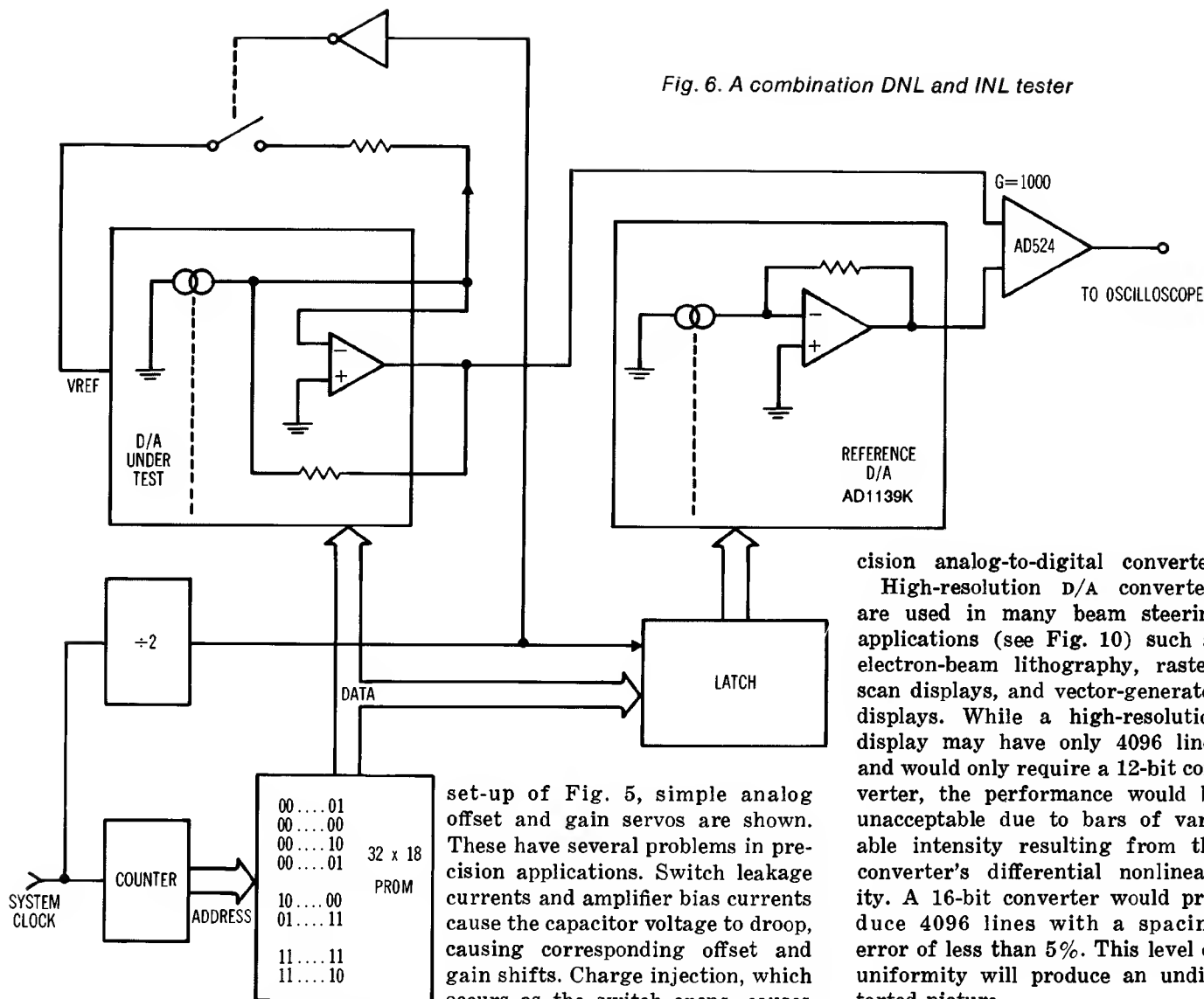


Fig. 6. A combination DNL and INL tester

pliance — the maximum voltage that can appear at the current output terminal while maintaining specified linearity. A more useful feature of a current output device is that the output amplifier can be custom tailored to the application. For example, a low drift amplifier could be used for precision applications, or a power amplifier could be used to provide a large output drive for a programmable power supply (see Fig. 8). The programmable power supply can be used to control the magnetic fields produced by the electromagnets in a cyclotron, as a voltage reference, or to test A/D converters in ATE systems.

A high resolution D/A converter is often used as a digitally controlled potentiometer for use in an auto zero or gain calibration circuit. In the integral linearity test

set-up of Fig. 5, simple analog offset and gain servos are shown. These have several problems in precision applications. Switch leakage currents and amplifier bias currents cause the capacitor voltage to droop, causing corresponding offset and gain shifts. Charge injection, which occurs as the switch opens, causes a step at the amplifier output resulting in similar offset and gain errors. The amplifier output constantly ramps up and down due to time delays throughout the circuit, mostly due to the RC time constant of the integrator. This, too, produces gain and offset shifts. All of these problems can be eliminated by replacing the amplifier and switch with a D/A converter and comparator (see Fig. 9). The offset converter is incremented until the converter under test is zeroed, and the gain converter is incremented until the converter under test is adjusted to full scale. The digital inputs are latched, and the correction voltages remain constant and jitter-free until the next auto zero or auto gain cycle. This same technique can be used to make a zero droop sample and hold, or a pre-

cision analog-to-digital converter.

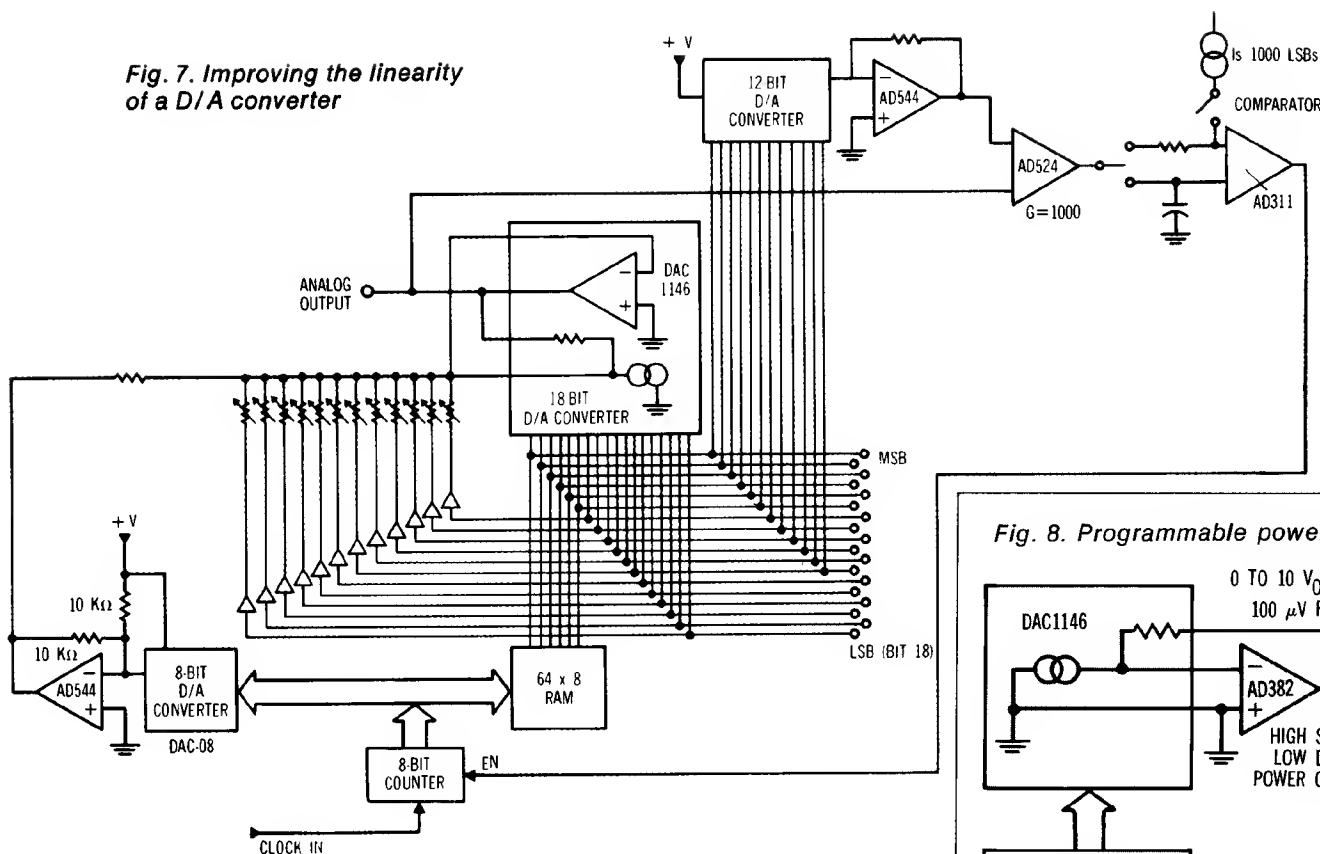
High-resolution D/A converters are used in many beam steering applications (see Fig. 10) such as electron-beam lithography, raster-scan displays, and vector-generated displays. While a high-resolution display may have only 4096 lines and would only require a 12-bit converter, the performance would be unacceptable due to bars of variable intensity resulting from the converter's differential nonlinearity. A 16-bit converter would produce 4096 lines with a spacing error of less than 5%. This level of uniformity will produce an undistorted picture.

#### D/A converters speed assembly

A growing area where high resolution converters are used is in manufacturing and automated assembly, for positioning of robot arms or precision machining (see Fig. 11). A computerized lathe or milling machine can produce a component of up to three feet in length with 0.0005-in. tolerances. A converter with at least 16 bits of resolution is needed to control the depth of cut as well as the horizontal position of the cut. Under microprocessor control, the horizontal positioning converter would be incremented to position the object, while the depth control converter would be adjusted to accurately and repeatedly set the depth of cut.

In multiplying D/A converters, the voltage reference can be varied.

**Fig. 7. Improving the linearity of a D/A converter**



The analog output is the product of the reference input and the digital input. Such converters can multiply in one, two, or four quadrants, depending on the allowed polarity of the voltage reference and the digital inputs.

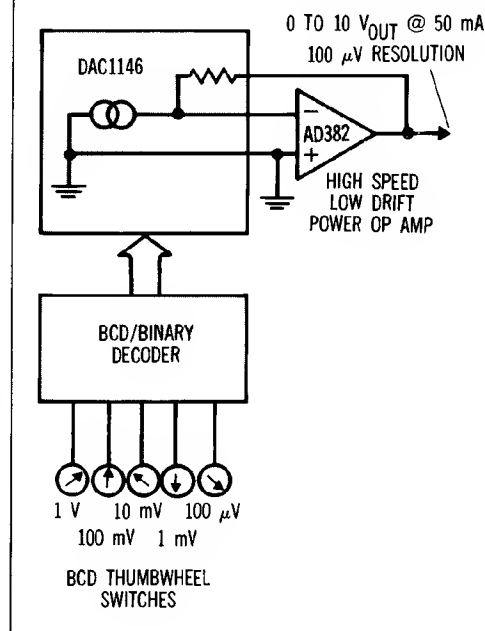
An interesting application for a high-resolution multiplying D/A converter is a digitally programmed resistor for use as a resistance temperature detector (RTD) simulator (see Fig. 12). For resolution and accuracy of  $0.1^{\circ}\text{C}$  over a  $-220$  to  $+850^{\circ}\text{C}$  range, an RTD simulator must be capable of varying from  $10$  to  $400\ \Omega$  with  $10\ \text{m}\Omega$  of resolution. This requires a 16-bit converter. The excitation current from the RTD meter may vary by  $\pm 5\%$ , so a multiplying converter must be used to maintain a constant resistance. The analog output is proportional to the excitation current and the digital input. As the excitation current increases, the reference voltage increases. This causes the

output and the excitation voltage to increase. The simulated resistance is just the excitation voltage divided by the excitation current; therefore, it's dependent only upon the digital input code value. The system simulates a resistance programmed via a digital source at the converter's inputs.

### Waveform reconstruction specs

Users of high-resolution D/A converters in waveform reconstruction applications are generally not concerned with differential nonlinearity or any of the other traditional specifications. Instead, a new and highly specialized set of specifications are required. This is largely because many converters used for waveform reconstruction are part of a larger system where a dynamic waveform is digitized and reconstructed. The user's only interest is that this process be completed with a minimum of error, exhibited in several ways, the most

**Fig. 8. Programmable power supply**

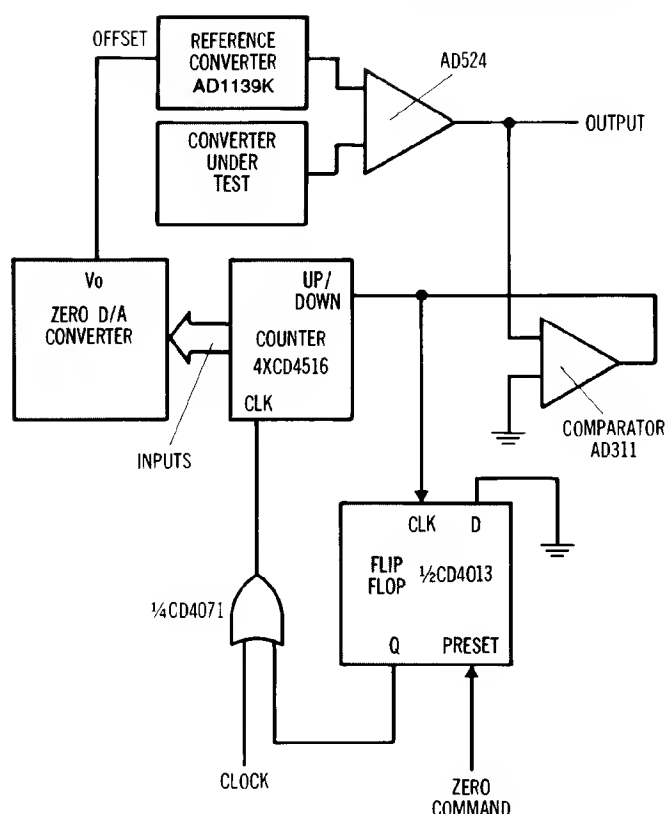


significant being total harmonic distortion. Other sources of error are intermodulation distortion, noise, limited dynamic range, poor settling time, and aliasing.

Dynamic range is the ratio of the smallest output signal (1 LSB) to the largest output signal (full scale) that a converter can produce. For an N-bit converter, full scale is equal to  $2^N$  LSBs. Theoretically, the dynamic range of an N-bit converter is  $6N\ \text{dB}$ . Converter noise, coupled with inaccuracies in the LSB weight, can reduce this theoretical dynamic range slightly.

Signal-to-noise ratio (S/N) is the

Fig. 9. Offset calibration



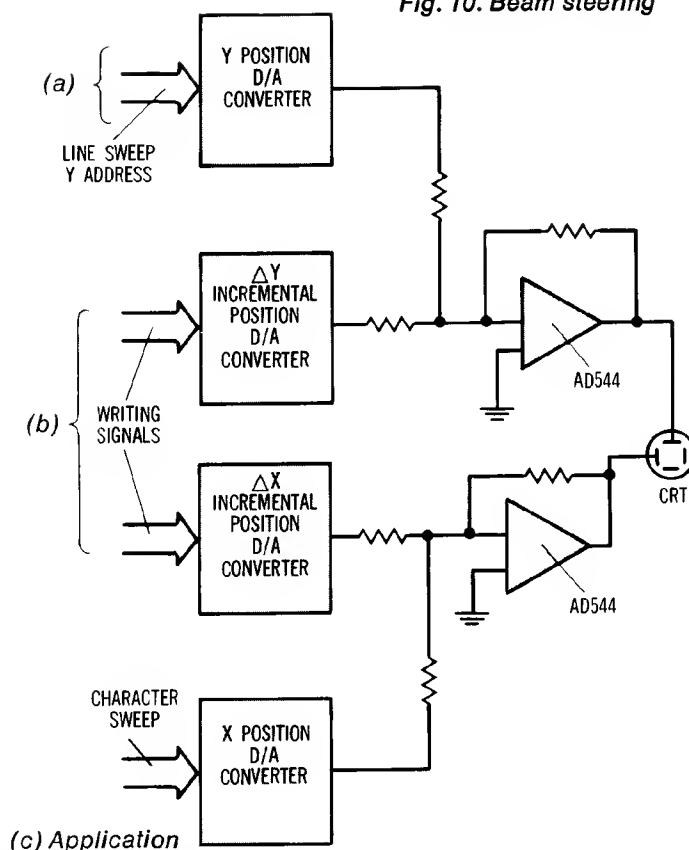
ratio of the maximum RMS signal to the RMS quantization error (see Fig. 13). The RMS value of the maximum sine wave that a converter can produce is the peak output divided by the square root of two, or  $Q \cdot 2^{N-1} / \sqrt{2}$ , where  $Q$  is defined to be the quantization interval. The quantization error increases linearly from  $-Q/2$  to  $+Q/2$  and then abruptly returns to  $-Q/2$ . The RMS value of this sawtooth wave is the peak output divided by the square root of three, or:  $Q / \sqrt{12}$ . The signal-to-noise ratio, then, is:  $2^N \sqrt{1.5}$ . This can be expressed in dB as  $S/N = 6.02N + 1.76$  dB.

Waveform reconstruction is a dynamic process and requires that the selected converter perform well in a dynamic sense. This means that the settling time must be faster than the time allotted by the process. (Settling time is the length of time between the switching of the digital inputs of the converter and the time when the output reaches and remains within a specified error band around its final value.)

Total harmonic distortion (THD) is the most important specification for a converter used for waveform generation or reconstruction. Roughly speaking, this is the difference between an ideal sine wave and a reconstructed version at the converter's output. THD is defined as the ratio of the square root of the sum of the squares of the RMS values of the harmonics to the RMS value of the fundamental. This means that the RMS energy of each harmonic must be squared and added together. The square root is taken and divided by the RMS energy of the fundamental. The result is the THD of the converter. For a converter with a finite number of digital inputs,  $N$ , and associated output voltages, THD can be calculated from the formula:

$$THD = \frac{RMS \text{ error}}{RMS \text{ signal}} = \sqrt{\frac{1}{N} \sum_{i=1}^N [E_L(i) + E_Q(i)]^2} \times 100\%$$

Fig. 10. Beam steering



(a) 11 lines of 4096 positioned with 12 bit accuracy. Note dark and light bars

(b) 11 lines of 4096 positioned with 16 bit accuracy. Note uniform bars

where  $E_L(i)$  is the linearity error of the converter at sampling point  $i$ , and  $E_Q(i)$  is the quantization error at sampling point  $i$ . Intermodulation distortion is caused by the additional error products produced when the ideal output is composed of two sine waves of different frequency.

When a D/A converter changes state, not all of its switches open and close simultaneously. Internal voltages and currents require finite times to reach their final values. In a CMOS converter, a large amount of charge is stored on the gate-to-source and gate-to-drain capaci-

tances of each switch. This charge is pumped to or from the analog output as the switches open and close. All of these effects combine to produce an output voltage or current spike, commonly known as a glitch. The amplitude of the glitch is nonlinearly related to the converter's input; thus, the glitch produces energy at harmonics of the fundamental frequency and causes harmonic distortion. When the analog output is asymmetric about zero volts, the second harmonic is generated. Asymmetric behavior of increasing or decreasing signals

generates third harmonics. Other asymmetric behavior will cause other harmonics (see Fig. 14).

### Eliminating the glitches

A deglitcher (see Fig. 15) is a special type of track-and-hold amplifier that holds the output constant from just before the input code changes, to just after the glitch has died out. It then acquires the new, stable output. The deglitcher generates its own output glitch, caused by charge injection from its switching circuits. But this glitch is usually small, of constant amplitude, and independent of the digital input code. It produces energy at the sampling frequency, not at the signal frequency or any of its harmonics, and therefore does not cause harmonic distortion. Band-limiting the deglitcher output with a fixed time constant suppresses distortion caused by slow rate limiting of the output amplifier.

Audio signals are inherently bi-

polar, and so the converter used to reconstruct them must be bipolar (see Fig. 16). One possible method for configuring such a device is to offset a standard binary converter by half scale. A second method is to sense the polarity of the signal and switch the output amplifier to either an inverter or a buffer as required. The remainder of the input determines the magnitude of the output voltage. Offset binary converters have a simple, clean architecture, and so can be made smaller, more reliable, and less expensive than a sign magnitude converter with the same performance. Alternatively, extra money can be spent on better resistor networks to yield an offset binary converter with improved performance over a sign magnitude device of the same price. For audio applications, however, a substantial amount of signal is around zero volts. An offset binary converter exhibits its worst temperature performance around zero volts because it counts on the MSB to track with the sum of all lesser significant bits, and with the bipolar offset resistor. A sign magnitude converter exhibits its best performance around zero volts because all bits are OFF. Good performance around zero is important because of the effect on S/N ratio. Large signals tend to mask error-induced noise, while small signals will be buried by the same noise. A binary converter with a current output can be converted to sign magnitude

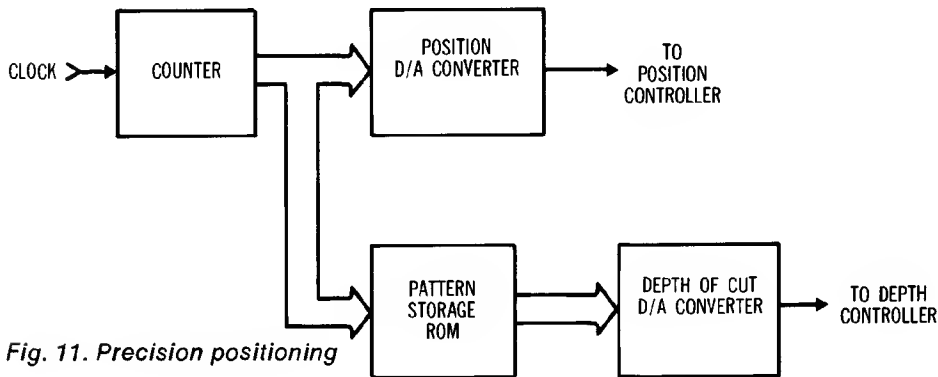
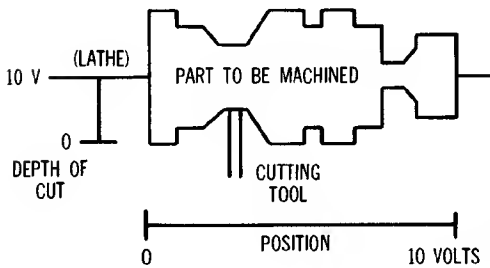


Fig. 11. Precision positioning

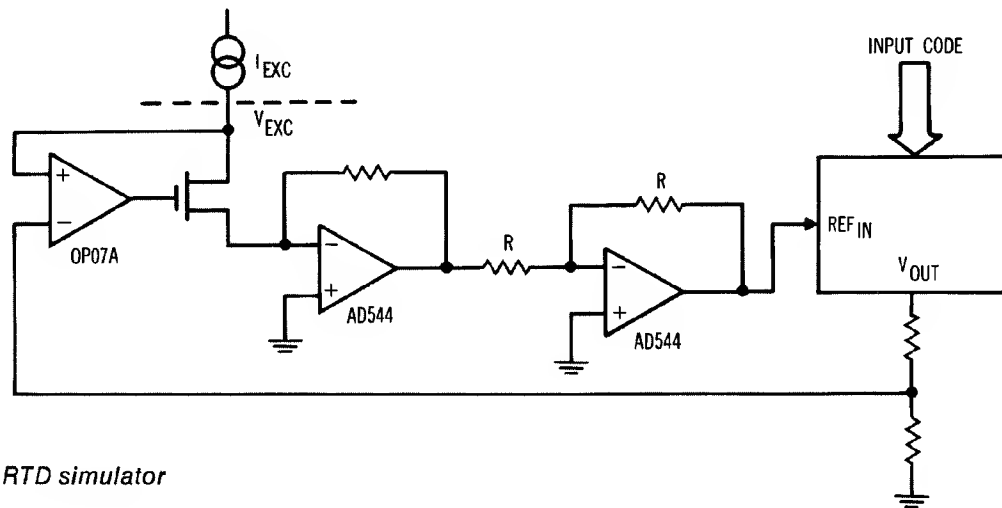
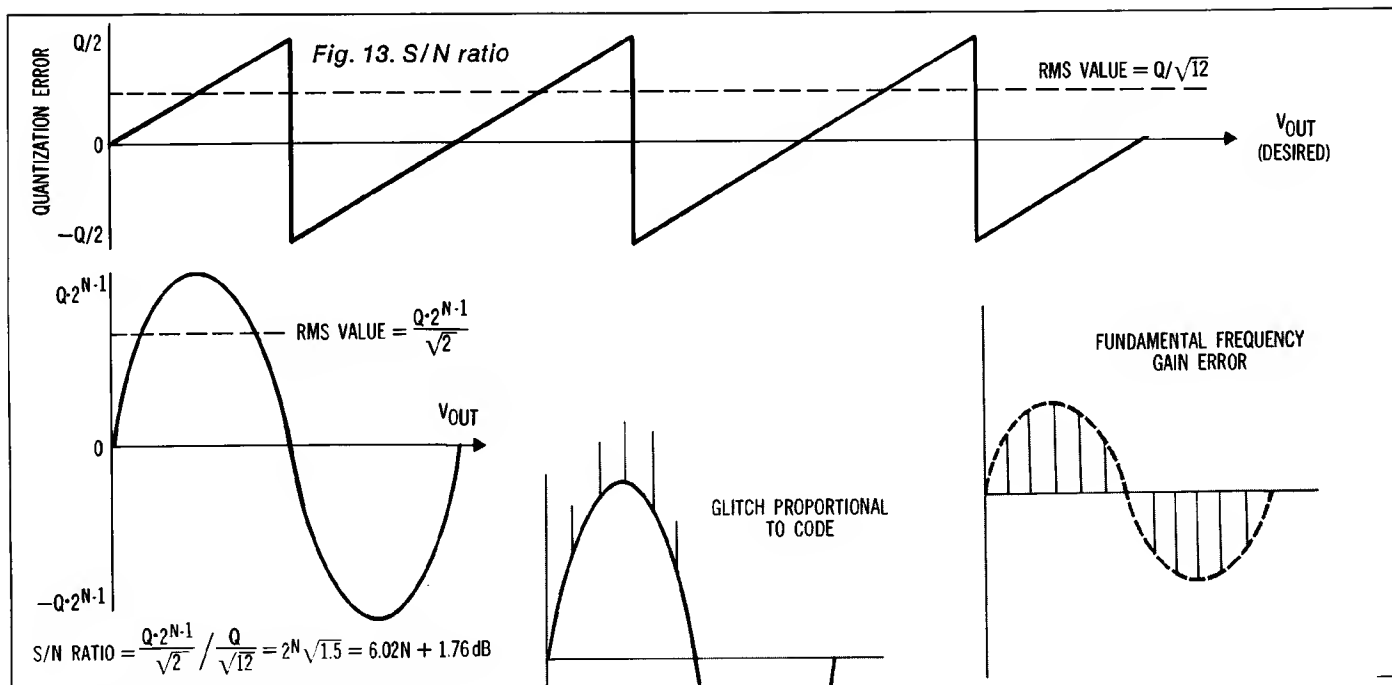


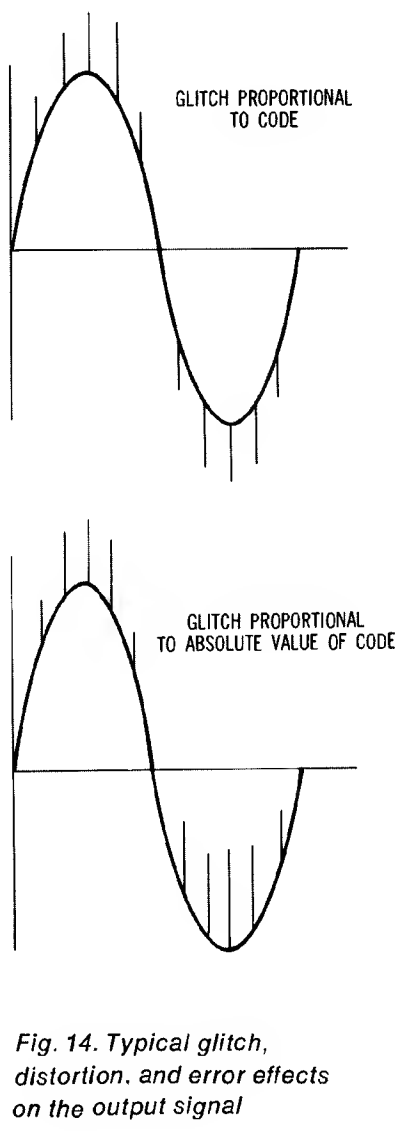
Fig. 12. RTD simulator



architecture by the addition of a low-drift amplifier, an SPDT CMOS switch, and an output buffer (see Fig. 17). The result is maximum DNL drift of  $\pm \frac{1}{2}$  ppm/ $^{\circ}\text{C}$  for  $\pm \frac{1}{8}$  full scale range and  $\pm 1$  ppm/ $^{\circ}\text{C}$  over the full scale range. Typical drifts are  $\pm \frac{1}{4}$  ppm/ $^{\circ}\text{C}$  around zero and  $\pm \frac{1}{2}$  ppm/ $^{\circ}\text{C}$  over the full range.

### Check total harmonic distortion

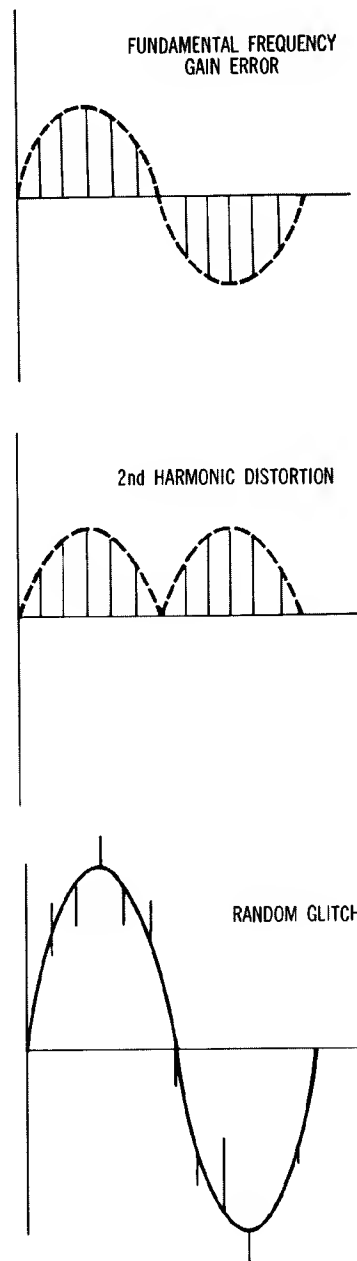
Total harmonic distortion can be tested using the circuit of Fig. 18. In this test set up, the PROM contains one cycle of a computer generated sine wave. Frequency select switches are used to program the adder with the number of codes that it should skip on each count. This series of sinusoidally-related digital codes is fed to the converter to generate a staircase approximation of an analog sine wave. If the adder is set to increase the PROM address by one on each count, 4096 inputs will be presented to the converter on each cycle through the PROM. If the adder is set to increase the PROM address by 1024 on each count, only four inputs will be presented on each cycle. In this way, any of 2048 discrete frequencies between 12 Hz and 25 kHz can be generated with a constant 50 kHz sampling rate. The D/A output (see Fig. 19) is deglitched and displayed on the spectrum analyzer. Total harmonic



*Fig. 14. Typical glitch, distortion, and error effects on the output signal*

distortion can be computed by comparing the amplitude of the fundamental frequency with the amplitudes of the harmonics as discussed.

A high resolution D/A converter



with good dynamics can be used as a precision function generator. Through microprocessor control, the converter can produce the standard output functions — sine waves, square waves, pulses, triangle

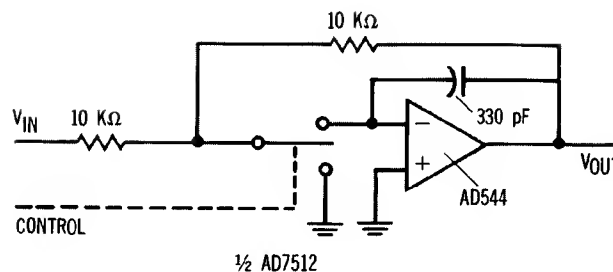
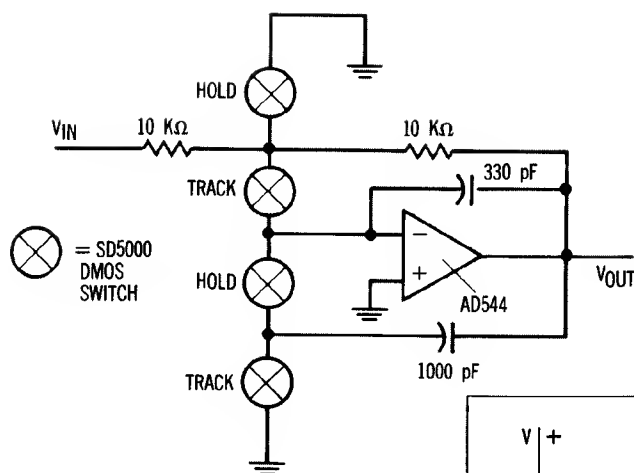


Fig. 15. Deglitcher circuits for D/A converters

offset, and inversion are controlled by appropriately scaling the inputs. Frequency and duty cycle are controlled by processor timing. More complex functions such as double pulses, bursts and pulse trains are also easily implemented. The real advantage of using a high resolution device as a function generator is that arbitrary waveforms can be generated. These can be used to simulate complex waveforms, to program test patterns, or to generate hyperbolic or other transcendental functions. A 16-bit converter with a settling time of less than  $5 \mu\text{s}$

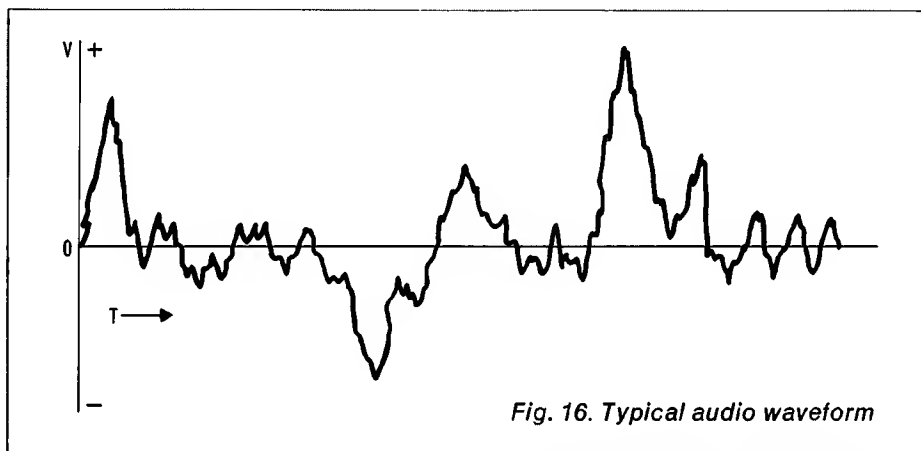


Fig. 16. Typical audio waveform

can produce outputs at up to 200 kHz with distortion of less than 0.002%.

A very high performance, reasonably low cost, two-channel digital audio system can be implemented by combining a fast, high-resolu-

tion converter with a track-and-hold amplifier and two deglitchers. This implementation allows a stereo pair of analog outputs to be simultaneously updated at 50 kHz. The track and hold stores the right-channel output while the left chan-

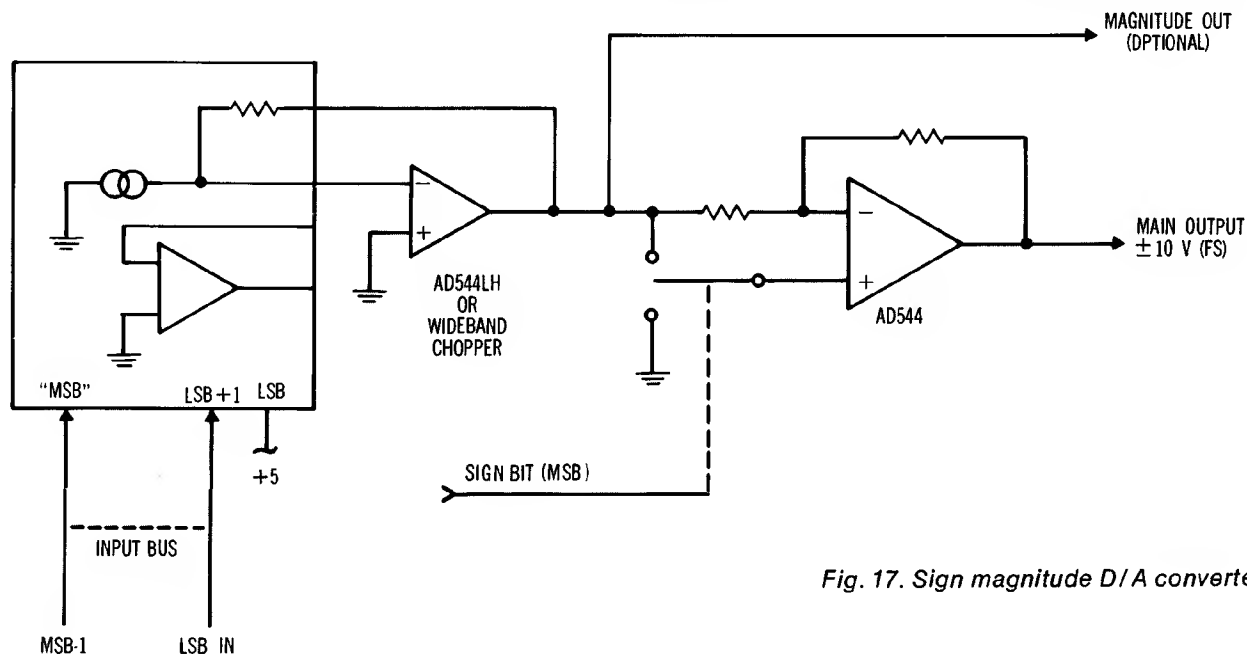
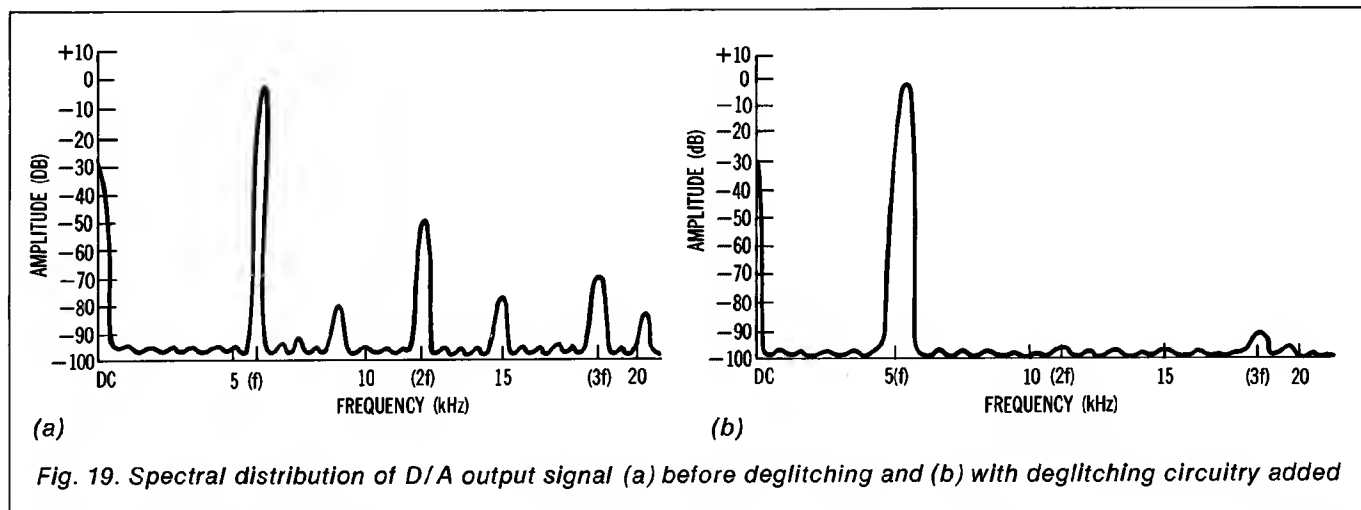


Fig. 17. Sign magnitude D/A converter



nel is presented to the input of the converter. The two deglitchers are then switched from the hold mode to the follow mode, and their outputs are switched from the previous sample to the new sample. The deglitcher response is bandlimited to eliminate distortion caused by slew rate limiting of the amplifier. A time constant of  $3.4 \mu\text{s}$  can ensure the passage of full-power 20 kHz sine waves without distortion. A 16-bit converter used along with a track-and-hold amplifier and deglitchers can produce an audio signal with distortion of less than 0.005%.

Telecommunications provides another major area of application for

high resolution converters. Data is digitized for transmission over telephone, broadcast, or satellite communications links and then reconstructed on the receiving end. Again, the significant parameters are THD and settling time, which limits the rate of transmission.

Other uses for high resolution converters in waveform reconstruction include sonar and seismic research. In sonar, a signal is transmitted and the time until it is reflected back to the receiver is measured. The time, stored in digital format, is presented to the converter. A picture of the ocean bottom is subsequently generated. In seismic research, a similar process

occurs. An explosive is detonated, and the vibrations are measured using A/D converters at specified locations. Data are processed by a computer, and presented to a D/A converter which is used to generate a seismic profile.

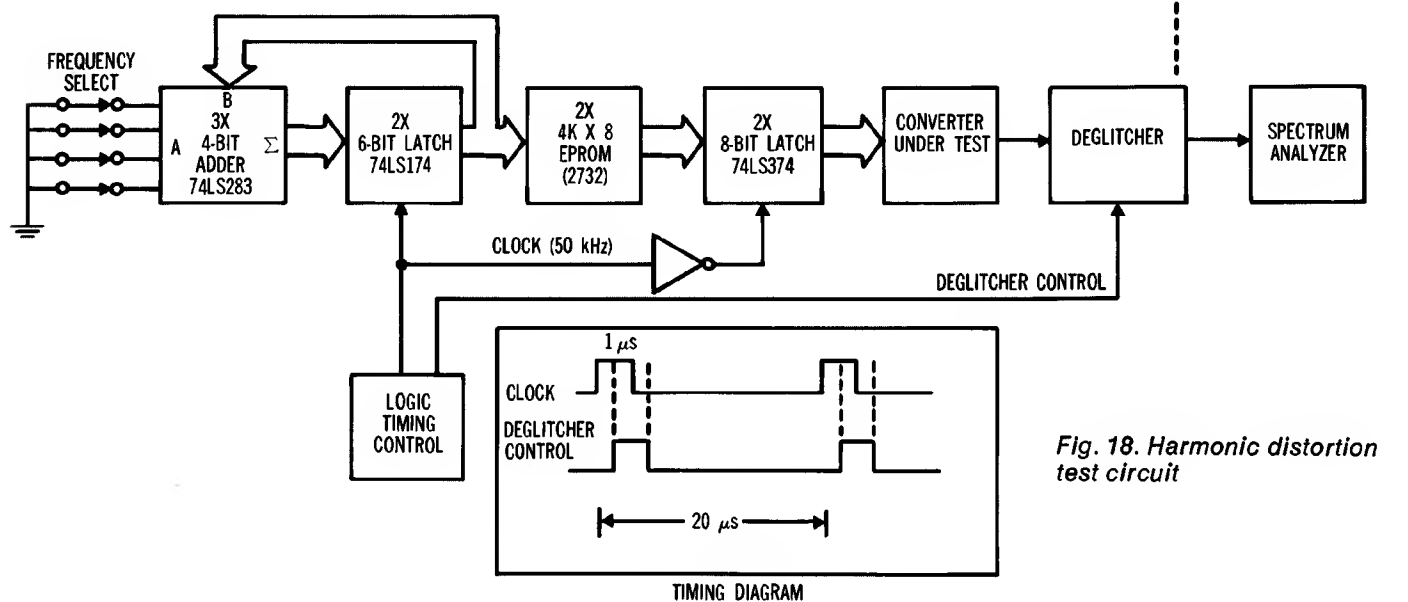


Fig. 18. Harmonic distortion test circuit

